UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/353,847	07/15/1999	HYUN CHANG LEE	8733/PD-6981	4171

30827 7590 09/10/2002

MCKENNA LONG & ALDRIDGE LLP
1900 K STREET, NW
WASHINGTON, DC 20006

EXAMINER
ANYASO, UCHENDU O

ART UNIT	PAPER NUMBER
2675	10

DATE MAILED: 09/10/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/353,847	Applicant(s) LEE ET AL.	
	Examiner Uchendu O Anyaso	Art Unit 2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 July 1999* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 July 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3, 7, 8* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. **Claims 1-26** are pending in this action.

Claim Rejections - 35 USC ' 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. **Claims 1-26** are rejected under 35 U.S.C. 102(b) as being anticipated by Sakaedani et al (EP Patent 0 881 622).

Regarding **independent claims 1** and **9**, and for **claims 4-8** and **10**, Sakaedani teaches a residual image eliminating apparatus for a liquid crystal display device by teaching a power-off screen clearing circuit for an active matrix liquid crystal display (column 6, lines 21-26; column 4, lines 18-22, 53-58 through column 5, lines 1-10; column 5, lines 52-58 through column 6, lines 1-9).

Furthermore, Sakaedani teaches a power-off screen clearing circuit for an active matrix LCD having active switching elements have structures in which many active switching elements are arranged in a matrix (*see Abstract,* column 1, lines 3-7).

Furthermore, Sakaedani teaches a level shifting means by teaching an afterimage circuit 35 for receiving a power supply voltage and a ground voltage (see column 6, lines 21-26; column 4, lines 18-22, 53-58 through column 5, lines 1-10; column 5, lines 52-58 through column 6, lines 1-9).

Regarding **claims 2** and **3,** in further discussion of claim 1, Sakaedani teaches how the first voltage level has a lower voltage level than a minimum value of the image signals (column 5, lines 5-20, figure 3 at 37).

Regarding **independent claims 11** and **19**, and for **claims 12-18, 20-26**, Sakaedani teaches a power-off screen clearing circuit for an active matrix LCD having active switching elements have structures in which many active switching elements are arranged in a matrix (*see Abstract,* column 1, lines 3-7).

Furthermore, Sakaedani teaches a voltage generator circuit (34) that generates output voltages for the gate line driver circuit (33) (figure 3 at 33, 34).

Also, Sakaedani teaches a voltage enhancing device by teaching an afterimage circuit (35) comprising a charge storage circuit (36), a p-channel transistor (37), a voltage supply circuit (38), and a voltage reducing circuit (39) (column 4, lines 40-43, figure 3 at 35-39) wherein the configuration of the circuitry causes the potential of the node A to rise by the charge stored in the capacitance C1, and that voltage is subsequently supplied to the gate line driver circuit (33) (*see* column 5, lines 34-46, figure 3 at 35-39; *see also* column 5, lines 11-20).

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Uchendu O. Anyaso whose telephone number is (703)

306-5934. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steve Saras, can be reached at (703) 305-9720.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Uchendu O. Anyaso

09/08/2002